SGM6501

12-Input, 9-Output Video Switch Matrix with Output Drivers, Input Clamp, and Bias Circuitry

GENERAL DESCRIPTION

The SGM6501 switch matrix provides flexible options for today's video applications. The 12 inputs that can be routed to any of 9 outputs. Each input can be routed to one or more outputs, but only one input can be routed to any one output. The input to output routing is controlled via an I^2C-compatible digital interface.

Each input supports an integrated clamp option to set the output sync tip level of video with sync to ~600mV. Alternatively, the input may be internally biased to center signals without sync (Chroma, Pb, Pr) at ~1.3V. These DC output levels are for the 6dB gain setting. Higher gain settings increase the DC output levels accordingly. The input clamp/bias mode is selected via I^2C. Unused outputs may be powered down to reduce power dissipation.

The SGM6501 is available in Green SSOP-28 and TSSOP-28 packages. It operates over an ambient temperature range of -40℃ to +85℃.

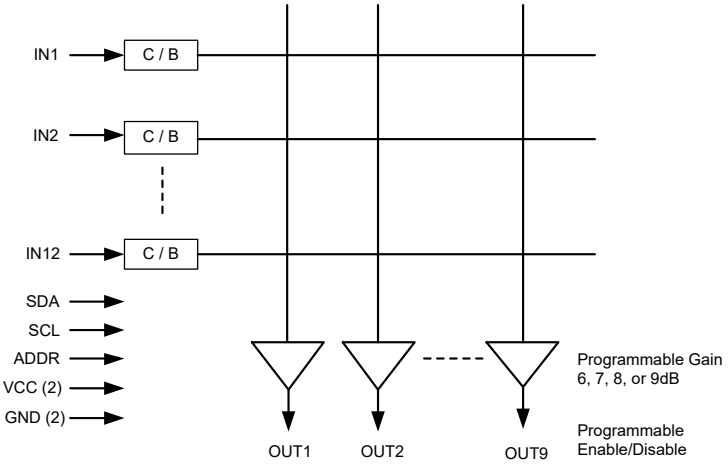
FEATURES

- **12 × 9 Crosspoint Switch Matrix**
- **One-to-One or One-to-Many Output Switching**
- **I^2C-Compatible Digital Interface, Standard Mode**
- **Supports SD, PS, and HD Video**
- **Input Clamp and Bias Circuitry**
- **Dual-Load (75Ω) Output Drivers with High-Impedance Disable**
- **Programmable Gain: 6dB, 7dB, 8dB, or 9dB**
- **AC- or DC-Coupled Inputs**
- **AC- or DC-Coupled Outputs**
- **Supply Voltage Range: 3.1V to 5.5V**
- **Available in Green SSOP-28 and TSSOP-28 Packages**

APPLICATIONS

Video Distribution
TV and HDTV Sets
Cable and Satellite Set-Top Boxes
A/V Switchers
Personal Video Recorders (PVR)
Security and Surveillance
Automotive (In-Cabin Entertainment)

BLOCK DIAGRAM

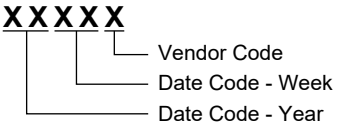


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6501	SSOP-28	-40℃ to +85℃	SGM6501YSS28G/TR	SGM6501 YSS28 XXXXX	Tape and Reel, 2000
	TSSOP-28	-40℃ to +85℃	SGM6501YTS28G/TR	SGM6501 YTS28 XXXXX	Tape and Reel, 2500

MARKING INFORMATION

XXXXX = Date Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage Range ..... -0.3V to 6V
Analog and Digital I/O ..... -0.3V to V_{CC} + 0.3V
Output Current Any One Channel, Do Not Exceed 40mA
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM (SSOP-28) 8000V
HBM (TSSOP-28) 7000V
CDM 2000V
MM 400V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

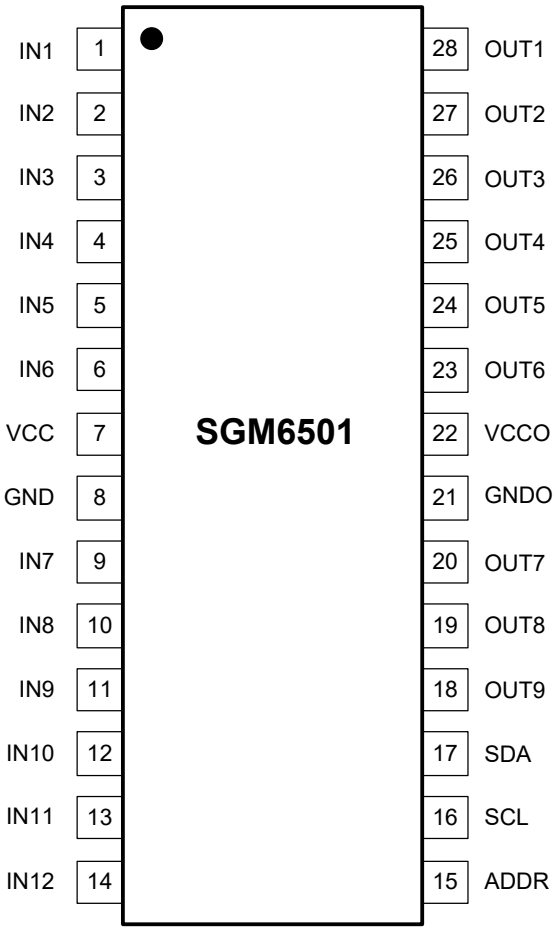
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

(TOP VIEW)



SSOP-28/TSSOP-28

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	IN1	Input. Channel 1.
2	IN2	Input. Channel 2.
3	IN3	Input. Channel 3.
4	IN4	Input. Channel 4.
5	IN5	Input. Channel 5.
6	IN6	Input. Channel 6.
7	VCC	Positive Power Supply.
8	GND	Ground.
9	IN7	Input. Channel 7.
10	IN8	Input. Channel 8.
11	IN9	Input. Channel 9.
12	IN10	Input. Channel 10.
13	IN11	Input. Channel 11.
14	IN12	Input. Channel 12.
15	ADDR	Selects I^2C Address. "0" = 0x06 (0000 0110) "1" = 0x86 (1000 0110)
16	SCL	Serial Clock for I^2C Port.
17	SDA	Serial Data for I^2C Port.
18	OUT9	Output. Channel 9.
19	OUT8	Output. Channel 8.
20	OUT7	Output. Channel 7.
21	GNDO	Ground.
22	VCCO	Positive Power Supply for Output Drivers.
23	OUT6	Output. Channel 6.
24	OUT5	Output. Channel 5.
25	OUT4	Output. Channel 4.
26	OUT3	Output. Channel 3.
27	OUT2	Output. Channel 2.
28	OUT1	Output. Channel 1.

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, V_{CC} = 5V, V_{IN} = 1V_{PP}, input bias mode, one-to-one routing, 6dB gain, all inputs AC-coupled with 0.1μF, unused inputs AC-terminated through 75Ω to GND, all outputs AC-coupled with 220μF into 150Ω loads, referenced to 400kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
General						
Supply Voltage Range	V_{CC}		3.1	5	5.5	V
DC Performance						
Video Output Range	V_{OUT}			2.8		V_{PP}
Supply Current	I_Q	No load, all outputs enabled		92	127	mA
DC Output Level	V_{clamp}	Clamp mode, input floating, 6dB gain setting		0.86		V
DC Output Level	V_{bias}	Bias mode, input floating, 6dB gain setting		1.3		V
Power Supply Rejection Ratio	PSRR	All channels, DC input = 0.5V		60		dB
Off Channel Output Impedance	R_{OFF}	Output disabled		3		kΩ
AC Performance						
Channel Gain Error	AV_{SD}	All channels, all gain setting, DC	-0.2	0	0.2	dB
Gain Step	AV_{STEP}	All channels, DC	0.9	1	1.1	dB
-1dB Bandwidth	f_{-1dB}	V_{OUT} = 1.4V_{PP}		59		MHz
-3dB Bandwidth	f_C	V_{OUT} = 1.4V_{PP}		84		MHz
Differential Gain	DG	V_{CC} = 5V, 4.43MHz		0.1		%
Differential Phase	DP	V_{CC} = 5V, 4.43MHz		0.3		°
SD Output Distortion	THD_{SD}	V_{OUT} = 1.4V_{PP}, 5MHz, V_{CC} = 5V		0.2		%
HD Output Distortion	THD_{HD}	V_{OUT} = 1.4V_{PP}, 22MHz, V_{CC} = 5V		0.9		%
Input Crosstalk	X_{TALK1}	1MHz, V_{OUT} = 2V_{PP}		-74		dB
	X_{TALK2}	15MHz, V_{OUT} = 2V_{PP}		-51		dB
Output Crosstalk	X_{TALK3}	1MHz, V_{OUT} = 2V_{PP}		-70		dB
	X_{TALK4}	15MHz, V_{OUT} = 2V_{PP}		-47		dB
Multi-Channel Crosstalk	X_{TALK5}	4.43MHz, V_{OUT} = 2V_{PP}		-52		dB
	X_{TALK6}	6.5MHz, V_{OUT} = 2V_{PP}		-49		dB
	X_{TALK7}	9MHz, V_{OUT} = 2V_{PP}		-47		dB
Signal-to-Noise Ratio	SNR_{SD}	NTC-7 weighting, 4.2MHz LP, 100kHz HP		77		dB
Channel Noise	V_{NOISE}	400kHz to 100MHz, input referred		20		nV/$\sqrt{Hz}$
Amplifier Recovery Time	AMP_{ON}	Post I^2C programming		200		ns

DIGITAL INTERFACE

The I^2C-compatible interface is used to program output enables, input to output routing, input clamp/bias, and output gain. The I^2C address of the SGM6501 is 0x06 (0000 0110) with the ability to offset it to 0x86 (1000 0110) by tying the ADDR pin high.

Both data and address data, of eight bits each, are written to the I^2C address to access all the control functions.

There are separate internal addresses for each output. Each output's address includes bits to select an input channel, adjust the output gain, and enable or disable the output amplifier. More than one output can connect to the same input channel for one-to-many routing. When the outputs are disabled, they are placed in a high-impedance state. This allows multiple SGM6501 devices to be paralleled to create a larger switch matrix. Typical output power-up time is less than 500ns.

The clamp/bias control bits are written to their own internal address, since they should always remain the same regardless of signal routing. They are set based on the input signal connected to the SGM6501.

All undefined addresses may be written without effect.

Output Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
Enable	1 bit	Write	0	7	Channel enable: 1 = Enable, 0 = Power Down (1)
Gain	2 bits	Write	0	6:5	Channel gain: 00 = 6dB, 01 = 7dB, 10 = 8dB, 11 = 9dB
INx	5 bits	Write	0	4:0	Input selected to drive this output: 00000 = OFF (2), 00001 = IN1, 00010 = IN2... 01100 = IN12

NOTES:

1. Power down places the output in a high-impedance state so multiple SGM6501 devices may be paralleled. Power down also de-selects any input routed to the specified output.
2. When all inputs are OFF, the amplifier input is tied to approximately 150mV and the output goes to approximately 300mV with the 6dB gain setting.

Output Control Register Map

Name	Address	Bit7	Bit6	Bit5	Bit4(1)	Bit3	Bit2	Bit1	Bit0
OUT1	0x01	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT2	0x02	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT3	0x03	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT4	0x04	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT5	0x05	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT6	0x06	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT7	0x07	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT8	0x08	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT9	0x09	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0

NOTE:

1. IN4 is provided for forward compatibility and should always be written as '0' in the SGM6501.

Clamp Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
Clmp	1 bit	Write	0	7:0	Clamp/Bias selection: 1 = Clamp, 0 = Bias

Clamp Control Register Map

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLAMP1	0x1D	Clmp8	Clmp7	Clmp6	Clmp5	Clmp4	Clmp3	Clmp2	Clmp1
CLAMP2	0x1E	Resv'd	Resv'd	Resv'd	Resv'd	Clmp12	Clmp11	Clmp10	Clmp9

I²C BUS CHARACTERISTICS

(T_A = +25℃, V_{CC} = 5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input Low	V_{IL}	SDA, SCL, ADDR	0		1.5	V
Digital Input High	V_{IH}	SDA, SCL, ADDR	3.0		V_{CC}	V
Clock Frequency	f_{SCL}	SCL		100		kHz
Input Rise Time	t_r	1.5V to 3V		1000		ns
Input Fall Time	t_f	1.5V to 3V		300		ns
Clock Low Period	t_{LOW}			4.7		μs
Clock High Period	t_{HIGH}			4.0		μs
Data Set-up Time	$t_{SU, DAT}$			300		ns
Data Hold Time	$t_{HD, DAT}$			0		ns
Set-up Time from Clock High to Stop	$t_{SU, STO}$			4		μs
Start Set-up Time Following a Stop	t_{BUF}			4.7		μs
Start Hold Time	$t_{HD, STA}$			4		μs
Start Set-up Time Following Clock Low to High	$t_{SU, STA}$			4.7		μs

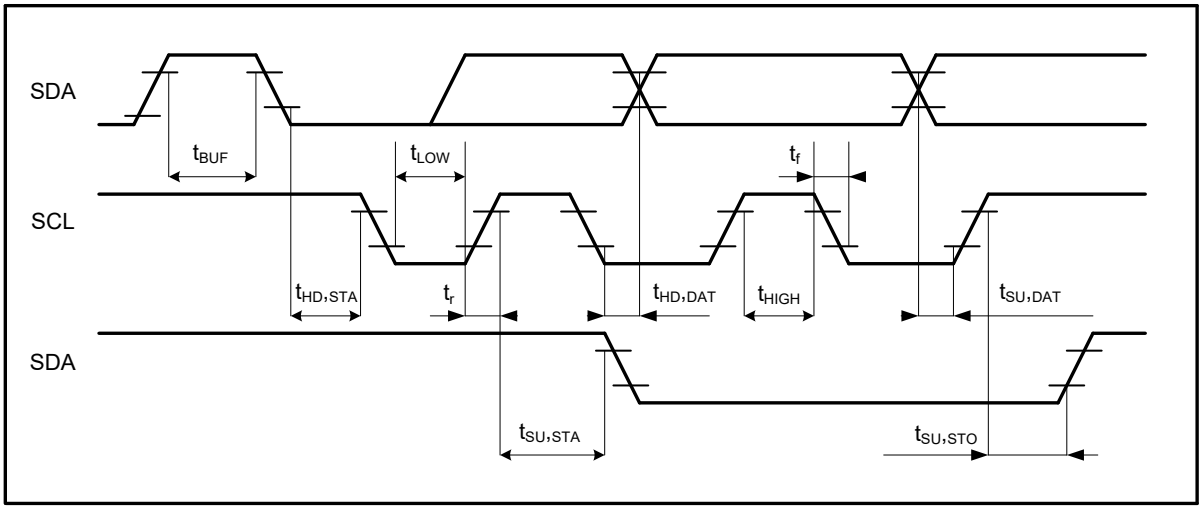


Figure 1. I²C Bus Timing

I²C INTERFACE

Operation

The I²C-compatible interface conforms to the I²C specification for standard mode. Individual addresses may be written, but there is no read capability. The interface consists of two lines: a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply through an external resistor. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Changes in the data line during this time are interpreted as control signals.

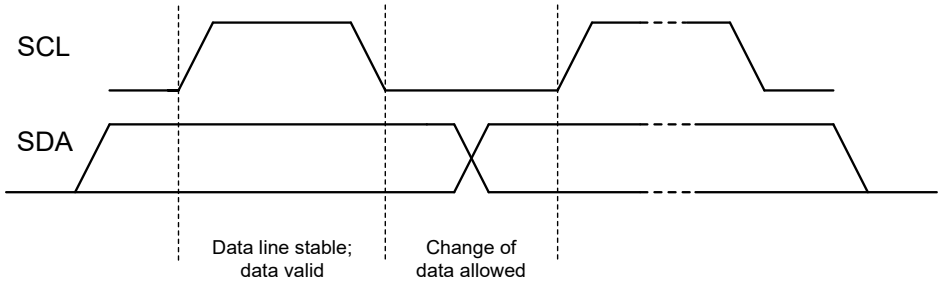


Figure 2. Bit Transfer

START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as START condition (S).

A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as STOP condition (P).

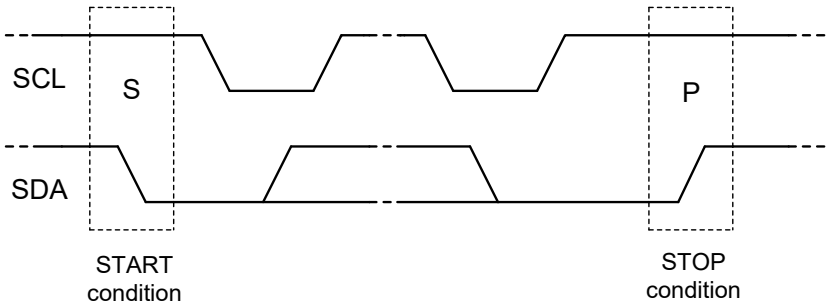


Figure 3. START and STOP Conditions

Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter while the master generates an extra acknowledge-related clock pulse. The slave receiver addressed must generate an acknowledge after the reception of each byte. A master receiver must generate an acknowledge after the reception of each byte clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

I²C INTERFACE (continued)

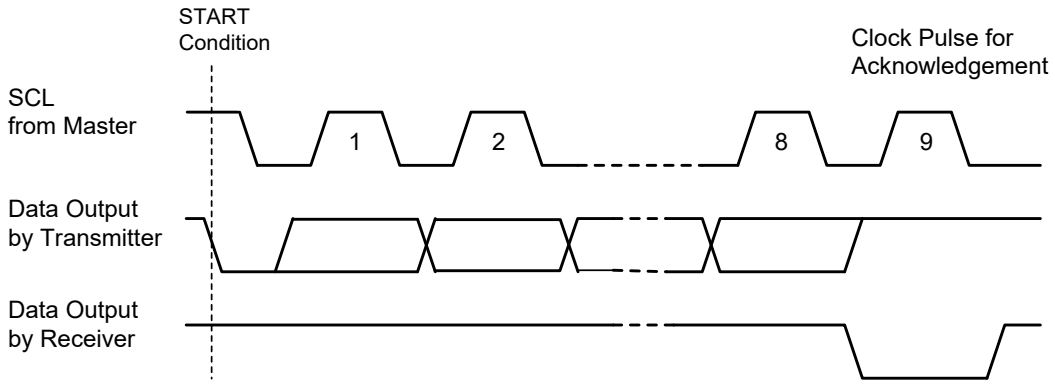


Figure 4. Acknowledgement on the I²C Bus

I²C Bus Protocol

Before any data is transmitted on the I²C bus, the device which is to respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C bus configuration for a data write to the SGM6501 is shown in Figure 5.

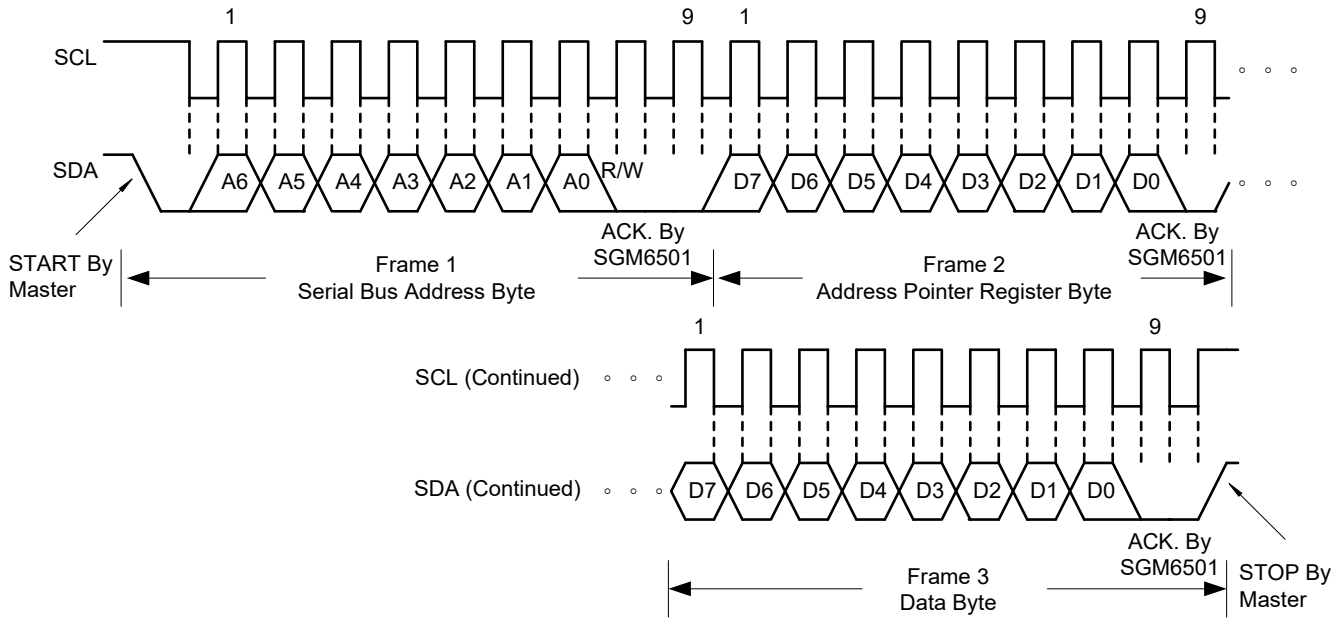


Figure 5. Write Register Address to Pointer Register; Write Data to Selected Register

APPLICATION NOTES

Input Clamp/Bias Circuitry

The SGM6501 can accommodate AC- or DC-coupled inputs.

Internal clamping and bias circuitry are provided to support AC-coupled inputs. These are selectable through the CLMP bits via the I^2C-compatible interface.

For DC-coupled inputs, the device should be programmed to use the 'bias' input configuration. In this configuration, the input is internally biased to 650mV through a 100kΩ resistor. Distortion is optimized with the output levels set between 250mV above ground and 500mV below the power supply. These constraints, along with the desired channel gain, need to be considered when configuring the input signal levels for input DC coupling.

With AC-coupled inputs, the SGM6501 uses a simple clamp rather than a full DC-restore circuit. For video signals with and without sync (Y, CV, R, G, B), the lowest voltage at the output pins is clamped to approximately 600mV above ground when the 6dB gain setting is selected.

If symmetric AC-coupled input signals are used (Chroma, Pb, Pr, Cb, Cr), the bias circuit can be used to center them within the input common range. The average DC value at the output is approximately 1.3V with a 6dB gain setting. This value changes depending upon the selected gain setting.

Gain Setting	Clamp Voltage	Bias Voltage
6dB	600mV	1.30V
7dB	660mV	1.50V
8dB	740mV	1.70V
9dB	840mV	1.90V

Figure 6 shows the clamp mode input circuit and the internally controlled voltage at the input pin for AC-coupled inputs.

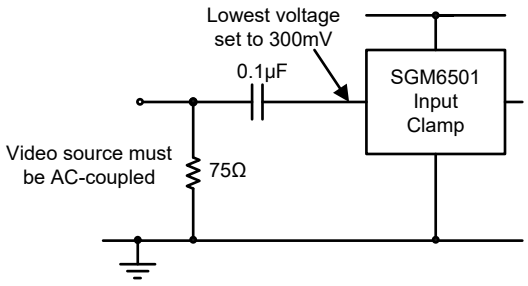


Figure 6. Clamp Mode Input Circuit

Figure 7 shows the bias mode input circuit and the internally controlled voltage at the input pin for AC-coupled inputs.

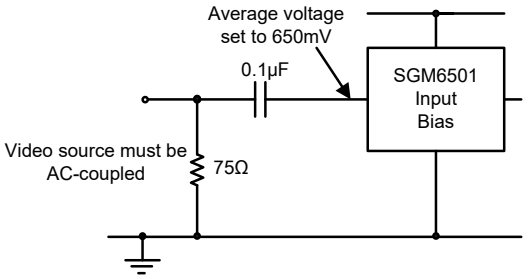


Figure 7. Bias Mode Input Circuit

Output Configuration

The SGM6501 outputs may be either AC or DC coupled. Resistive output loads can be as low as 75Ω, representing a dual, doubly terminated video load. High impedance, capacitive loads up to 20pF can also be driven without loss of signal integrity. For standard 75Ω video loads, a 75Ω matching resistor should be placed in series to allow for a doubly terminated load. DC-coupled outputs should be connected as shown in Figure 8.

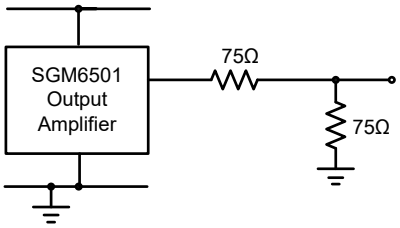


Figure 8. DC-Coupled Load Connection

If multiple low-impedance loads are DC coupled, increased power and thermal issues need to be addressed. In this case, the use of a multilayer board with a large ground plane to help dissipate heat is recommended. If a two-layer board is used under these conditions, an extended ground plane directly under the device is recommended. This plane should extend at least 0.5 inches beyond the device. PC board layout issues are covered in the Layout Considerations section.

Configure AC-coupled loads as shown in Figure 9.

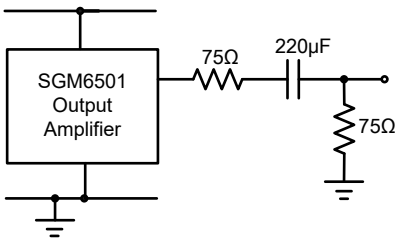


Figure 9. AC-Coupled Load Connection

APPLICATION NOTES (continued)

Thermal issues are significantly reduced with AC-coupled outputs, alleviating special PC layout requirements.

Each of the outputs can be independently powered down and placed in a high-impedance state with the ENABLE bit. This function can be used to mute video signals, to parallel multiple SGM6501 outputs, or to save power. When the output amplifier is disabled, the high-impedance output presents a 3kΩ load to ground. The output amplifier typically enters and recovers from the power down state in less than 300ns after being programmed.

When an output channel is not connected to an input, the input to that channel's amplifier is forced to approximately 150mV. The output amplifier is still active unless specifically disabled by the I^2C interface. Voltage output levels depend on the programmed gain for that channel.

Crosstalk

Crosstalk is an important consideration when using the SGM6501. Input and output crosstalks represent the two major coupling modes that may be present in a typical application. Input crosstalk is crosstalk in the input pins and switches when the interfering signal drives an open switch. It is dominated by inductive coupling in the package lead frame between adjacent leads. It decreases rapidly as the interfering signal moves further away from the pin adjacent to the input signal selected. Output crosstalk is coupling from one driven output to another active output. It decreases with increasing load impedance as it is caused mainly by ground and power coupling between output amplifiers. If a signal is driving an open switch, its crosstalk is mainly input crosstalk. If it is driving a load through an active output, its crosstalk is mainly output crosstalk.

Input and output crosstalk measurements are performed with the test configuration shown in Figure 10.

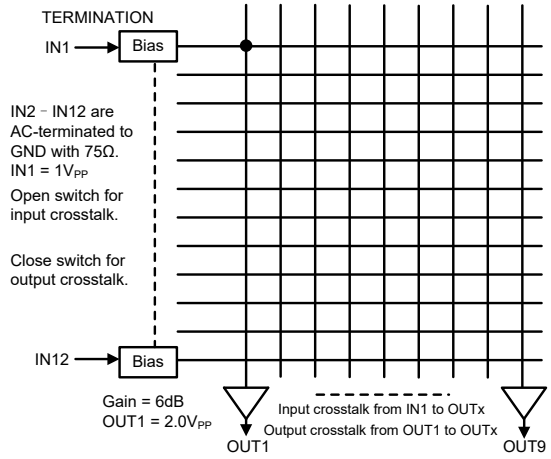


Figure 10. Test Configuration for Crosstalk

For input crosstalk, the switch is open and all inputs are in bias mode. Channel 1 input is driven with a $1V_{PP}$ signal, while all other inputs are AC-terminated with 75Ω. All outputs are enabled and crosstalk is measured from IN1 to any output.

For output crosstalk, the switch is closed. Crosstalk from OUT1 to any output is measured.

Crosstalk from multiple sources into a given channel is measured with the setup shown in Figure 11. Input IN1 is driven with a $1V_{PP}$ pulse source and connected to outputs OUT1 to OUT8. Input IN9 is driven with a secondary, asynchronous gray field video signal and is connected to OUT9. All other inputs are AC-terminated with 75Ω. Crosstalk effects on the gray field are measured and calculated with respect to a standard $1V_{PP}$ output measured at the load.

If not all inputs and outputs are needed, avoid using adjacent channels, where possible, to reduce crosstalk. Disable all unused channels to further reduce crosstalk and power dissipation.

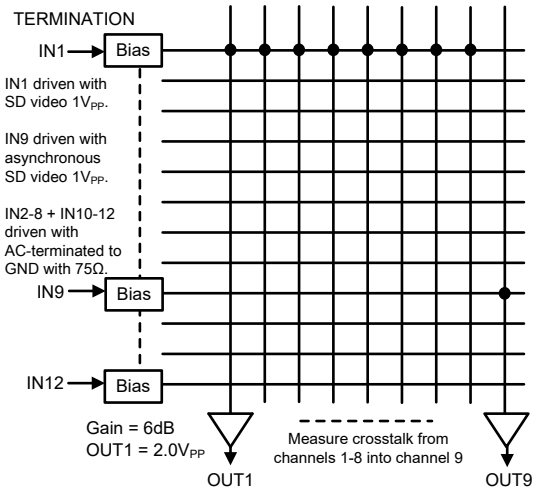


Figure 11. Test Configuration for Multi-Channel Crosstalk

Layout Considerations

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. SGMICRO offers a demonstration board to guide layout and aid device evaluation. The demo board is a four layers board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules listed below.

APPLICATION NOTES (continued)

Recommended Routing/Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Traces should run on top of the ground plane at all times.
- No trace should run over ground/power splits.
- Avoid routing at 90-degree angles.
- Minimize clock and video data trace length differences.
- Include 10μF and 0.1μF ceramic power supply bypass capacitors.
- Place the 0.1μF capacitor within 0.1 inches of the device power pin.
- Place the 10μF capacitor within 0.75 inches of the device power pin.
- For multilayer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device body by at least 0.5 inches on all sides. Include a metal paddle under the device on the top layer.
- Minimize all trace lengths to reduce series inductance.

Thermal Considerations

Since the interior of most systems, such as set-top boxes, TVs and DVD players, are at +70℃, consideration must be given to providing an adequate heat sink for the device package for maximum heat dissipation. When designing a system board, determine how much power each device dissipates. Ensure that devices of high power are not placed in the same location, such as directly above (top plane) or below (bottom plane) each other on the PCB.

PCB Thermal Layout Considerations

- Understand the system power requirements and environmental conditions.
- Maximize thermal performance of the PCB.
- Consider using 70μm of copper for high-power designs.
- Make the PCB as thin as possible by reducing FR4 thickness.
- Use vias in power pad to tie adjacent layers together.
- Remember that baseline temperature is a function of board area, not copper thickness.
- Modeling techniques can provide a first-order approximation.

Power Dissipation

Worst-case, additional die power due to DC loading can be estimated at $V_{CC}^2/4R_{load}$ per output channel. This assumes a constant DC output voltage of $V_{CC}/2$. For 5V V_{CC} with a dual DC video load, add 25/ (4×75) = 83mW, per channel.

Applications for the SGM6501 Video Switch Matrix

The increased demand for consumer multimedia systems has created a large challenge for system designers to provide cost-effective solutions to capitalize on the growth potential in graphics display technologies. These applications require cost-effective video switching and filtering solutions to deploy high-quality display technologies rapidly and effectively to the target audience. Areas of specific interest include HDTV, media centers, and automotive infotainment (such as navigation, in-cabin entertainment, and back-up cameras). In all cases, the advantages the integrated video switch matrix provides are high-quality video switching specific to the application, as well as video input clamps and on-chip, low impedance output cable drivers with switchable gain.

Generally the largest application for a video switch is for the front-end of an HDTV. This is used to take multiple inputs and route them to their appropriate signal paths (main picture and picture-In-picture, or PIP). These are normally routed into ADCs that are followed by decoders. Technologies for HDTV include LCD, plasma, and CRT, which have similar analog switching circuitry.

An example of a HDTV application is shown in Figure 12. This system combines a video switch matrix and two three-channel switchable anti-aliasing filters. There are two three-channel signal paths in the system; one for the main picture, the other for "Picture In Picture" (PIP).

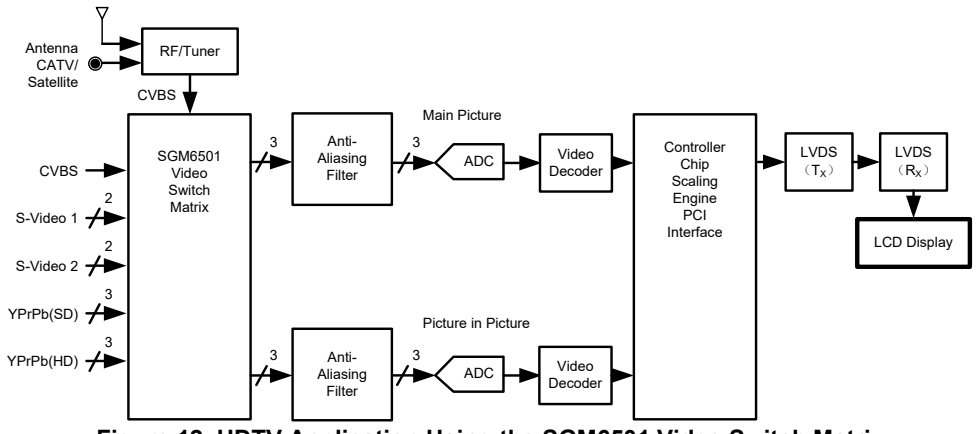


Figure 12. HDTV Application Using the SGM6501 Video Switch Matrix

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JANUARY 2013 – REV.A.3 to REV.A.4	Page
Added Recommended Land Pattern Information	13, 14
Added Tape and Reel Information	15, 16

MAY 2011 – REV.A.2 to REV.A.3	Page
Updated Package Description	All

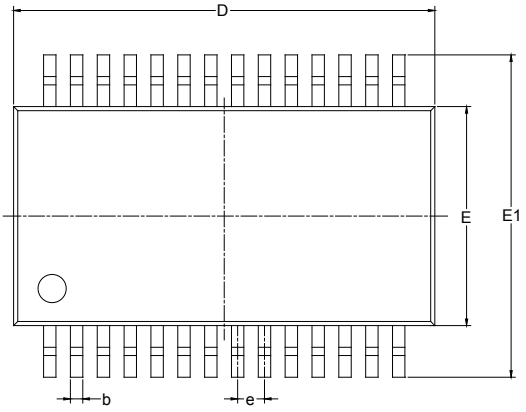
MARCH 2011 – REV.A.1 to REV.A.2	Page
Updated Package Outline Dimensions section	13
Added Tape and Reel Information	10, 11

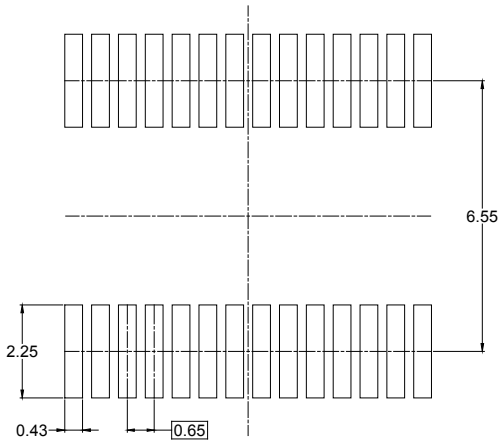
JANUARY 2011 – REV.A to REV.A.1	Page
Updated Pin Configurations section	3

Changes from Original (NOVEMBER 2010) to REV.A	Page
Changed from product preview to production data	All

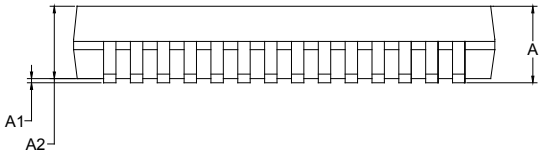
PACKAGE OUTLINE DIMENSIONS

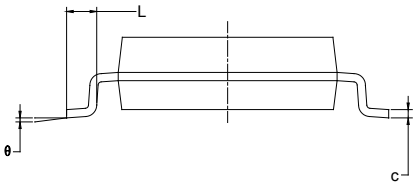
SSOP-28





RECOMMENDED LAND PATTERN (Unit: mm)

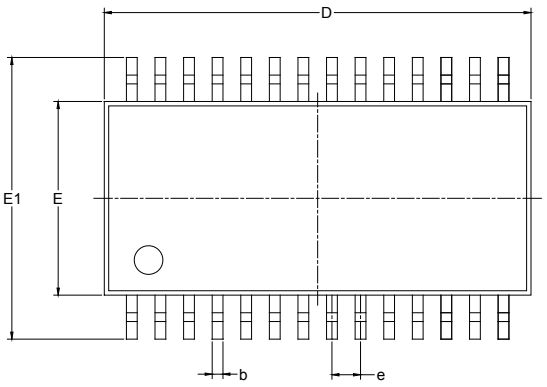


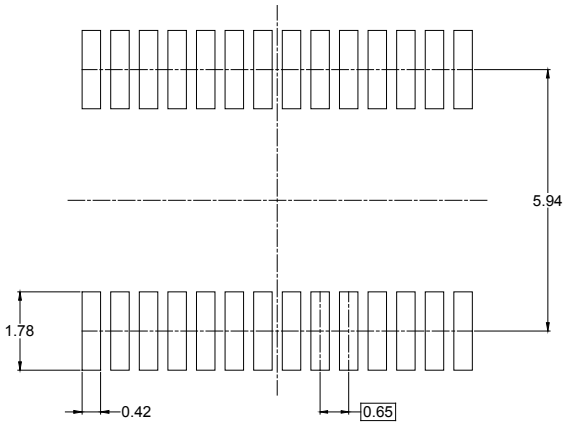


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		2.000		0.079
A1	0.050		0.002	
A2	1.650	1.850	0.065	0.073
b	0.220	0.380	0.009	0.015
c	0.090	0.250	0.004	0.010
D	9.900	10.500	0.390	0.413
E	5.000	5.600	0.197	0.220
E1	7.400	8.200	0.291	0.323
e	0.65 BSC		0.026 BSC	
L	0.550	0.950	0.022	0.037
θ	0°	8°	0°	8°

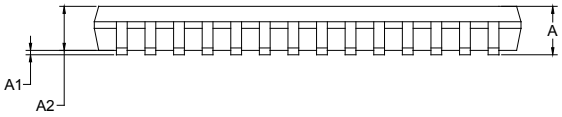
PACKAGE OUTLINE DIMENSIONS

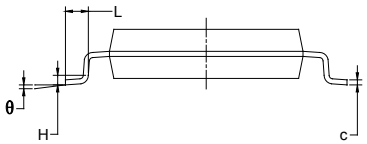
TSSOP-28





RECOMMENDED LAND PATTERN (Unit: mm)

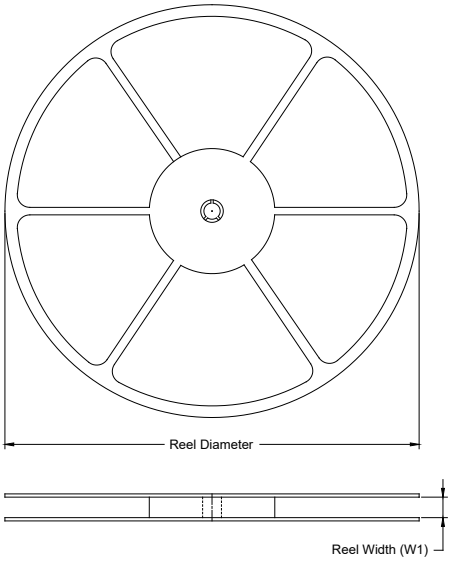




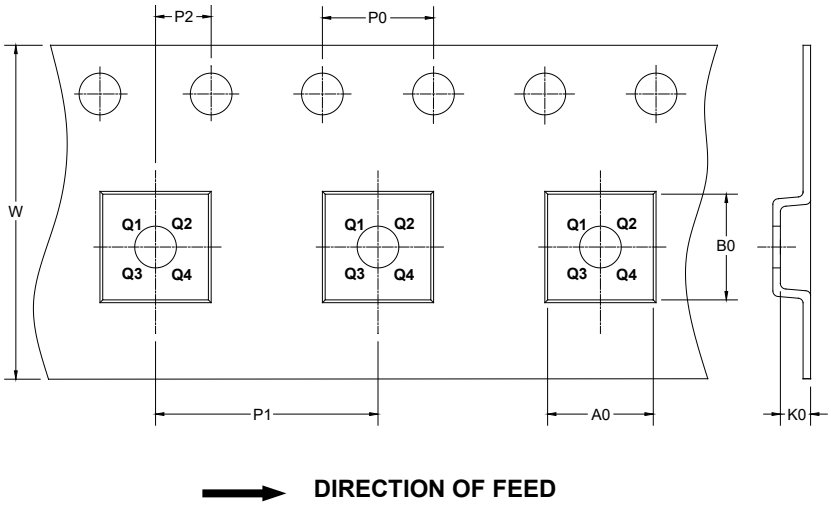
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.100		0.043
A1	0.020	0.150	0.001	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

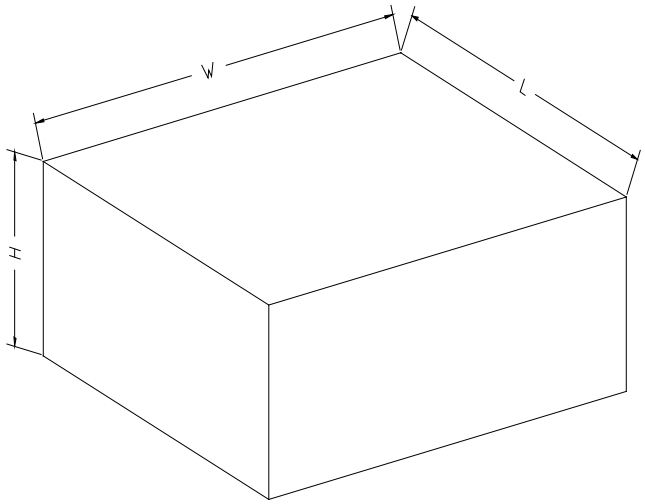
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SSOP-28	13″	16.4	8.20	10.50	0.30	4.0	12.0	2.0	16.0	Q1
TSSOP-28	13″	16.4	6.80	10.25	1.60	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002